providing a drive circuit including a single ferroelectric gate FET. In an exemplary embodiment, the scanning line in a two-dimensional matrix selectively scans a ferromagnetic gate FET directly.

With regard to the cited references, Applicant would emphasize that Nakai teaches complementary n-channel and p-channel ferroelectric gate transistors 104, 105. The activation of the transistors is indirectly driven by a pixel selecting transistor 101. Col. 14, lines 29-38. A liquid crystal 106 can be selectively driven by the first data signal or second data signal. The two states are stored by the ferroelectric substance provided in transistors 104, 105. This obviates the need to apply an alternating voltage to a supply line in the event there is no picture change, resulting in lower power consumption. Col. 15, lines 26-36. Significantly, Nakai specifically teaches away from the structure illustrated in Fig. 7 of the reference, illustrating a conventional display circuit. Col. 1, lines 37-52. The conventional arrangement, including a normal FET 93 directly connected to a scan line 92 and with a drain/source connected to a LCD 94 and storage capacitor 96. Nakai specifically criticizes the structure of Fig.7 for high power consumption.

Okumura teaches the exact arrangement of Fig. 7 in Nakai.

The Examiner cites the combination of Nakai and Okumura to teach each feature of the independent claim 2. The Examiner acknowledges that Nakai includes two ferroelectric gate transistors and further apparently concedes that Nakai does not teach use of a single ferroelectric gate transistor per pixel. The Examiner cites Okumura to teach the use of single transistor per pixel. The Examiner's rejection is completely without merit for at least four reasons.

First, the Examiner has provided no motivation to combine the teachings of Nakai and Okumura. The Examiner contends that it would be obvious to combine the references because the references purportedly each relate to two dimensional matrix display devices. While references must be drawn from analogous art in order to combine their features, this is not a sufficient condition for modifying teachings of the art. Here, the Examiner has failed to provide the motivation, even assuming arguendo, that the references are drawn from analogous art.

Second, the express teachings of Nakai clearly teach away from its combination with Okumura. In fact, Fig. 1 of Okumura corresponds exactly to the type of circuit of Fig.7 of Nakai, which the Nakai reference criticizes for requiring high driving power.

Third, as previously discussed in the record, Nakai relies on the complementary nature of n-channel and p-channel ferromagnetic gate transistors to provide the objects of the invention. A single transistor per pixel would defeat the principle of operation of Nakai. In effect, provision of the single pixel would likely require the application of an alternating voltage even in the event that there is no signal change.

Fourth, as a related matter, while the Examiner cites Okumura to teach generally the use of a single FET for a drive circuit, the drive circuit of Okumura corresponds to a normal FET and not a ferroelectric gate FET. The teachings of the single FET indicates no teachings for the ferroelectric gate FET. Applicant would emphasize that Okumura requires complementary FETs that would tend to teach away from a single ferroelectric FET described in the independent claims. Therefore, claims 2, 4, 5, 6, 8, 10 and 11 are patentable for at least these reasons.

With further regard to claims 6 and 14, Applicant would request that the Examiner provide a proper reference to show the equivalence between binary static drive and the drive for

a multigradation display device. The recent decision of In re Lee, 61 USPQ2d 1430, 1435 (Fed. Cir. 2002) has severely limited the extent to which an Examiner may rely on well-known information to one skilled in the art to support a rejection. Applicant would maintain that the rejection of claims 6 and 14, describing the binary static drive, is improper as it has no evidentiary support.

With further regard to claims 28-34, these claims describe the direct connection between a ferroelectric gate and a data line. The Examiner correctly concedes that Nakai does not teach this feature. While the Examiner appears to offer a rationale why a second transistor would be obvious, the Examiner offers no supporting reference or rationale as to why the direct connection would be obvious. As discussed above, In re Lee severely limits the instances where reliance on unsupported assertions can be used in making a rejection. The Examiner's rationale with regard to claims 28-34 on the direct connections is without merit.

In view of the above, Applicant submits that claims 2-6, 8-16 and 18-34 are in condition for allowance. Therefore it is respectfully requested that the subject application be passed to issue at the earliest possible time. The Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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